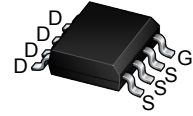


Description

The TX4435S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

General Features

$V_{DS} = -30V$ $I_D = -9A$

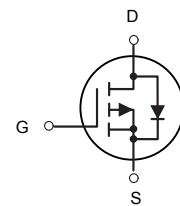
$R_{DS(ON)} < 20m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 30	V
V_{GS}	Gate-Source Voltage	+ 20	V
$I_D@T_A=25^{\circ}C$	Drain Current ³ , V_{GS} @ 10V	-9	A
$I_D@T_A=70^{\circ}C$	Drain Current ³ , V_{GS} @ 10V	-7.3	A
IDM	Pulsed Drain Current ¹	-50	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/°C
TSTG	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	50	°C/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-7A	-	18	20	mΩ
		V _{GS} =-4.5V, I _D =-5A	-	32	36	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-7A	-	16	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V	-	-	-30	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =-7A	-	18	29	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-24V	-	3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	10	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =-15V	-	8	-	ns
t _r	Rise Time	I _D =-1A	-	6.6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	44	-	ns
t _f	Fall Time	V _{GS} =-10V	-	34	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1175	1690	pF
C _{oss}	Output Capacitance	V _{DS} =-25V	-	195	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	190	-	pF
V _{SD}	Forward On Voltage ²	I _S =-2.1A, V _{GS} =0V	-	-	-1.2	V
t _{rr}	Reverse Recovery Time	I _S =-7A, V _{GS} =0V, dI/dt=100A/μs	-	28	-	ns
Q _{rr}	Reverse Recovery Charge		-	18	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t_≤10sec ; 125 °C/W when mounted on Min. cop

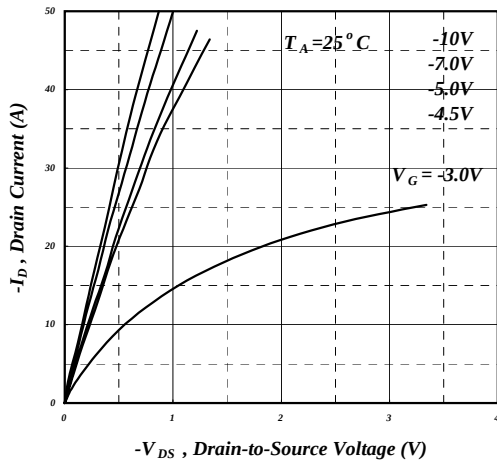


Fig 1. Typical Output Characteristics

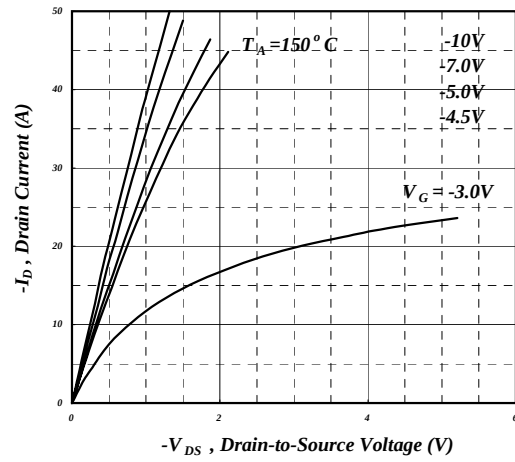


Fig 2. Typical Output Characteristics

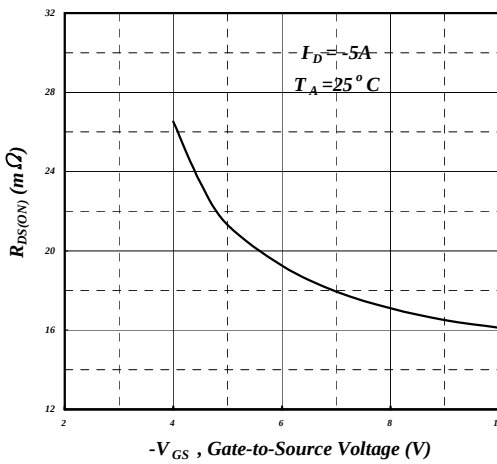
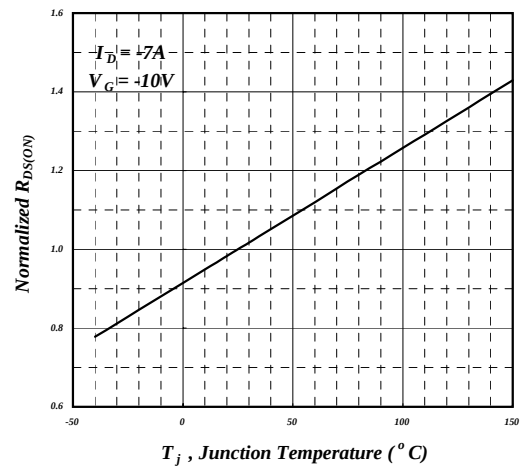
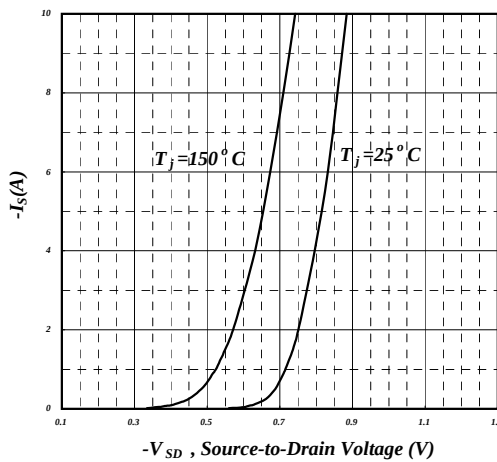


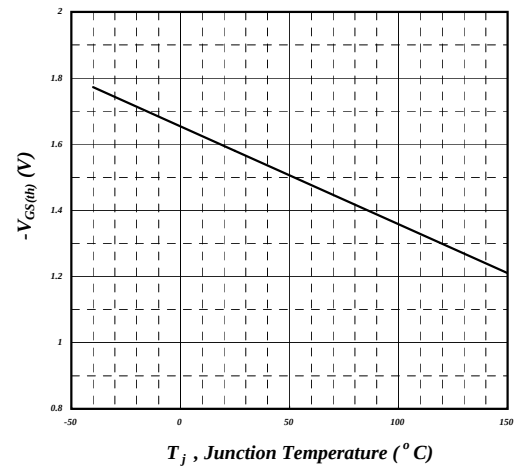
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

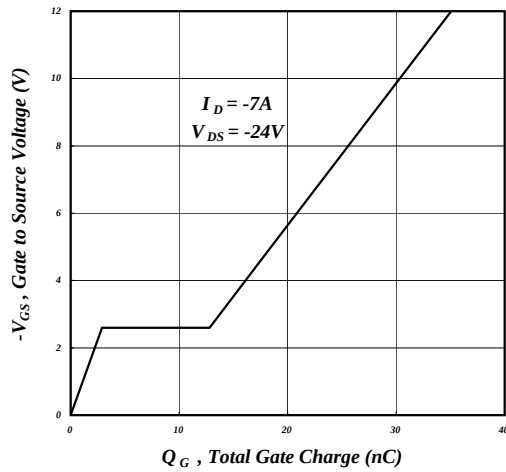


Fig 7. Gate Charge Characteristics

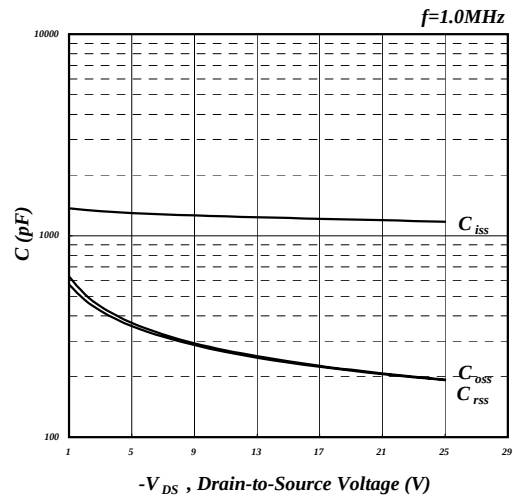


Fig 8. Typical Capacitance Characteristics

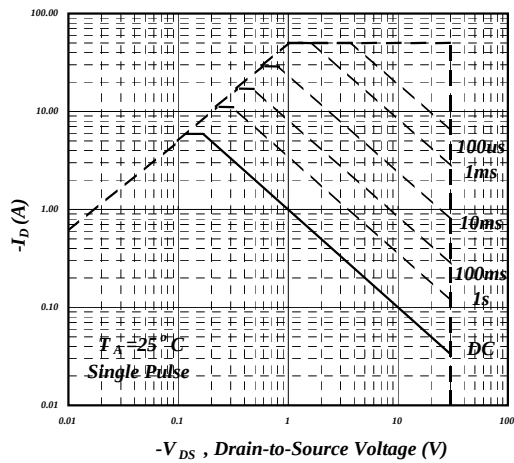


Fig 9. Maximum Safe Operating Area

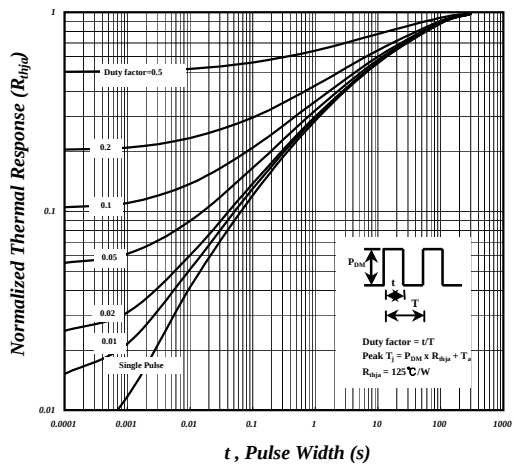


Fig 10. Effective Transient Thermal Impedance

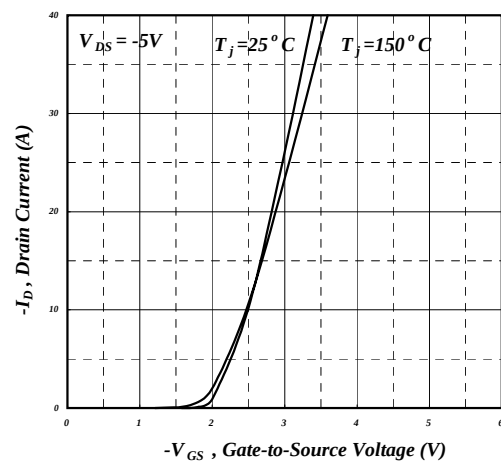


Fig 11. Transfer Characteristics

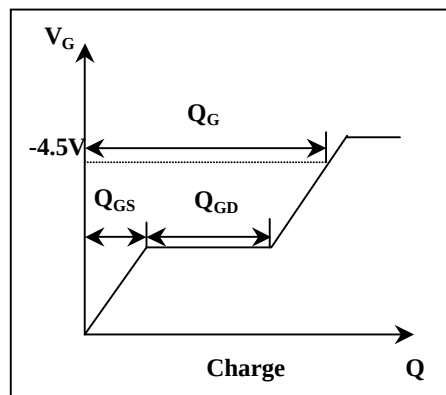
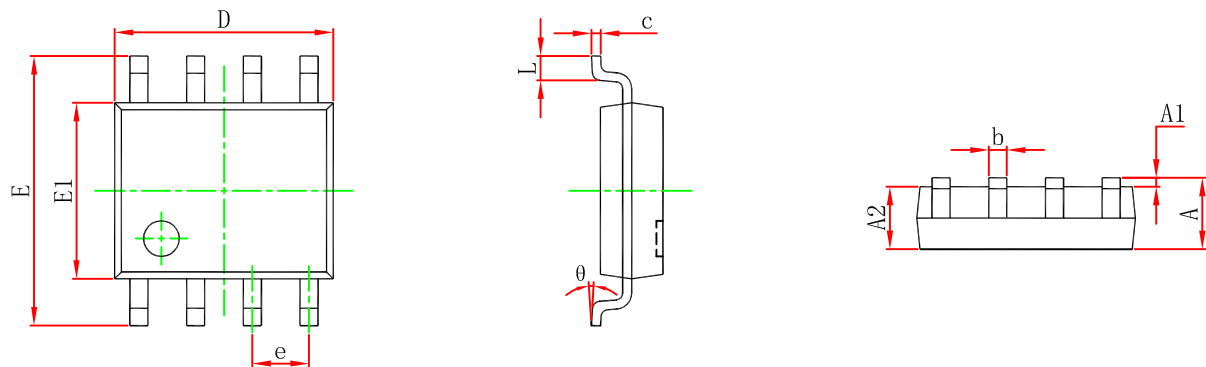
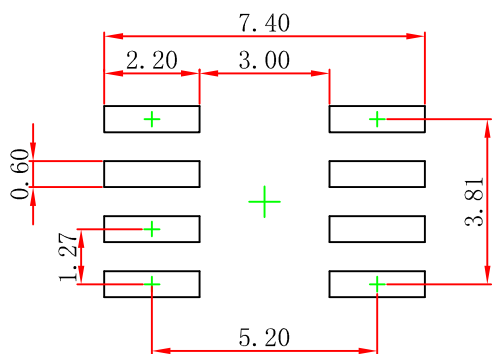


Fig 12. Gate Charge Circuit

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

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